

CLAIMS

We Claim:

1 1. In a data storage device having one or more media
2 surfaces, a corresponding number of at least read devices, a
3 spindle motor for moving the one or more media surfaces, an
4 actuator for moving the at least read devices relative to the one
5 or more media surfaces, a read device preamplifier, coupled to the
6 at least read devices, a servo control coupled to the actuator, for
7 driving the actuator in response to control signals, an integrated
8 data storage device controller integrated circuit comprising:
9 a host interface for interfacing with a host computer;
10 at least one internal communications and control bus, for
11 transferring stored data and control data to and from elements
12 within the integrated data storage device controller and
13 interconnected with the host interface to transfer stored data and
14 control data to and from the integrated data storage device
15 controller;
16 a read device data processor, coupled to the read device
17 preamplifier and the at least one internal communications and
18 control bus, for receiving and processing read device data from the
19 read device preamplifier;

20 a motion control servo logic, coupled to the at least one
21 internal communications and control bus, and to the servo control,
22 for generating control signals for driving the servo control;

23 a disc controller, coupled to the at least one internal
24 communications bus, for transferring stored data to the host
25 interface; and

26 a microcontroller, coupled to the at least one internal
27 communications bus, for generating control data to control devices
28 within the integrated data storage device controller integrated
29 circuit.

0
1
2
3
4
5
TOP SECRET//
REF ID: A6516666

1 2. The integrated data storage device controller integrated
2 circuit of claim 1, wherein the data storage device comprises an
3 optical disc drive, the one or more media surfaces comprises an
4 optical disc, and the corresponding number of at least read devices
5 comprises a laser.

1 3. The integrated data storage device controller integrated
2 circuit of claim 2, wherein the optical disc drive comprises a CD-
3 ROM drive and the optical disc comprises a CD-ROM.

1 4. The integrated data storage device controller integrated
2 circuit of claim 2, wherein the optical disc drive comprises a DVD
3 drive, and the optical disc comprises a DVD.

1 5. The integrated data storage device controller integrated
2 circuit of claim 2, wherein the optical disc drive comprises a
3 compact disc drive, and the optical disc comprises a compact disc.

1 6. The integrated data storage device controller integrated
2 circuit of claim 2, wherein the optical disc drive comprises a CD-R
3 drive, and the optical disc comprises a CD-R.

1 7. The integrated data storage device controller integrated
2 circuit of claim 2, wherein the optical disc drive comprises a CD-
3 RW drive, and the optical disc comprises a CD-RW.

1 8. The integrated data storage device controller integrated
2 circuit of claim 1, wherein the data storage device comprises a
3 floppy disk drive, the one or more media surfaces comprises a

4 magnetic floppy disk, and the corresponding number of at least read
5 devices comprises a read/write head.

1 9. The integrated data storage device controller integrated
2 circuit of claim 1, wherein the data storage device controller
3 integrated circuit is rendered in complimentary Metal Oxide
4 Semiconductor (CMOS) transistor circuitry.

1 10. The integrated data storage device controller integrated
2 circuit of claim 1, further comprising:

3 a digital signal processor, coupled to the at least one
4 internal communications bus, for processing raw stored data from
5 the read device data processor and outputting processed stored
6 data.

1 11. The integrated data storage device controller integrated
2 circuit of claim 10, wherein said microcontroller comprises:

3 a microprocessor having a set of instructions for controlling
4 a data storage device; and

5 an internal memory for storing a first speed critical portion
6 of microprocessor code and data containing instructions for

7 processing, retrieving, and storing data to and from the data
8 storage device,

9 wherein the microprocessor accesses an external memory through
10 the at least one internal communications bus to access a second
11 non-speed critical portion of microprocessor code and data
12 containing instructions not related to processing, retrieving, and
13 storing date to and from the data storage device.

12. The integrated data storage device controller integrated
1 circuit of claim 11, wherein said at least one internal
2 communications bus comprises:

3 a microcontroller local bus coupled to said microprocessor and
4 said internal memory for transferring the microprocessor code and
5 data to and from the microprocessor;

6 a peripheral bus coupled to said microprocessor with said read
7 device data processor and at least read device data processor, said
8 motion control servo logic, said disc drive controller, and said
9 digital signal processor;

10 an external memory bus, coupled to said microprocessor and an
11 external memory, for transferring microprocessor code and data to
12 and from said microprocessor; and

14 a bus/memory controller, coupled to and interfacing said
15 microcontroller local bus, said peripheral bus, and said external
16 memory bus.

1 13. The integrated data storage device controller integrated
2 circuit of claim 12, wherein a first portion of elements are
3 provided as hard design blocks, and a second portion of elements
4 are provided as soft design blocks such that the soft block
5 components may be readily redesigned without redesigning the hard
6 block components in order to customize the integrated data storage
7 device controller integrated circuit.

1 14. The integrated data storage device controller integrated
2 circuit of claim 1, wherein said internal communications bus
3 further comprises:

4 a MUX for selectively multiplexing outputs of one or more of
5 the disc controller, the microprocessor, and the read device data
6 processor with one or more I/O pins such that the integrated
7 circuit may selectively output signals from one or more of the of
8 the disc controller, the microprocessor, the read device data
9 processor.

1 15. The integrated data storage device controller integrated
2 circuit of claim 1, wherein said internal communications bus
3 further comprises:

4 a MUX for selectively multiplexing outputs of one or more of
5 the disc controller, the microprocessor, and the read device data
6 processor with one or more I/O pins such that the integrated data
7 storage device controller integrated circuit may selectively
8 operate as a discrete disc controller, component microprocessor,
9 and read device data processor.

16. A data storage device comprising:

one or more media surfaces;

a number of at least read devices corresponding to the one or more media surfaces;

a spindle motor for moving the one or more media surfaces;

an actuator for moving the at least read devices relative to media surfaces;

a read device preamplifier, coupled to the number of at least read devices;

a servo control coupled to the actuator, for driving the actuator in response to control signals; and

an integrated data storage device controller integrated circuit comprising:

14 at least one internal communications and control bus, for
15 transferring stored data and control data to and from elements
16 within the integrated data storage device controller and with
17 a host interface to transfer stored data and control data to
18 and from the integrated data storage device controller;

19 a read device data processor, coupled to the read device
20 preamplifier and the at least one internal communications and
21 control bus, for receiving and processing read device data
22 from the read device preamplifier;

23 a motion control servo logic, coupled to the servo
24 control, for generating control signals for driving the servo
25 control;

26 a disc controller, coupled to the at least one internal
27 communications bus, for transferring stored data to the host
28 interface; and

29 a microcontroller, coupled to the at least one internal
30 communications bus, for generating control data to control
31 devices within the integrated data storage device controller
32 integrated circuit.

17. The data storage device of claim 16, wherein the data storage device comprises an optical disc drive, the one or more

media surfaces comprises an optical disc, and the corresponding number of at least read devices comprises a laser.

1 18. The data storage device of claim 17, wherein the optical
2 disc drive comprises a CD-ROM drive and the optical disc comprises
3 a CD-ROM.

1 19. The data storage device of claim 17, wherein the optical
2 disc drive comprises a DVD drive, and the optical disc comprises a
3 DVD.

1 20. The data storage device of claim 17, wherein the optical
2 disc drive comprises a compact disc drive, and the optical disc
3 comprises a compact disc.

1 21. The data storage device of claim 17, wherein the optical
2 disc drive comprises a CD-R drive, and the optical disc comprises
3 a CD-R.

1 22. The data storage device of claim 17, wherein the optical
2 disc drive comprises a CD-RW drive, and the optical disc comprises
3 a CD-RW.

23. The data storage device of claim 16, wherein the data storage device comprises a floppy disk drive, the one or more media surfaces comprises a magnetic floppy disk, and the corresponding number of at least read devices comprises a read/write head.

1 24. The data storage device of claim 16, wherein the data storage device controller integrated circuit is rendered in
2 complimentary Metal Oxide Semiconductor (CMOS) transistor
3 circuitry.

1 25. The data storage device of claim 24, wherein said integrated data storage device controller integrated circuit further comprises:

4 a digital signal processor, coupled to the at least one
5 internal communications bus, for processing raw stored data from
6 the read device data processor and outputting processed stored
7 data.

1 26. The data storage device of claim 25, wherein said
2 microcontroller comprises:

3 a microprocessor having a limited command set of instructions
4 optimized for controller a data storage device; and

5 an internal memory for storing a first portion of
6 microprocessor code containing instructions for processing,
7 retrieving, and storing data to and from the data storage device,

8 wherein the microprocessor accesses an external memory through
9 the at least one internal communications bus to access a second
0 portion of microprocessor code containing instructions not related
1 to processing, retrieving, and storing date to and from the data
2 storage device.

1 27. The data storage device of claim 26, wherein said at
2 least one internal communications bus comprises:

3 a microcontroller local bus coupled to said microprocessor and
4 said internal memory for transferring the microprocessor code and
5 data to and from the microprocessor;

6 a peripheral bus coupled to said microprocessor with said read
7 device data processor, said motion control servo logic, said disc
8 drive controller, and said digital signal processor;

9 an external memory bus, coupled to said microprocessor and an
10 external memory, for transferring microprocessor code and data to
11 and from said microprocessor; and

12 a bus/memory controller, coupled to and interfacing said
13 microcontroller local bus, said peripheral bus, and said external
14 memory bus.

1 28. The data storage device of claim 27, wherein said read
2 device data processor, said microprocessor, and said internal
3 memory are provided as hard design blocks, and said disc controller
4 and servo controller are provided as soft design blocks such that
5 the soft block components may be readily redesigned without
6 redesigning the hard block components in order to customize the
7 integrated data storage device controller integrated circuit.

1 29. The data storage device of claim 28, wherein said
2 internal communications bus further comprises:

3 a MUX for selectively multiplexing outputs of the disc
4 controller, the microprocessor, and the read device data processor
5 with one or more I/O pins such that the integrated data storage
6 device controller integrated circuit may selectively operate as a

7 discrete disc controller, component microprocessor, a read device
8 data processor.

TOP SECRET//
REF ID: A6512

1 30. In a data storage device having one or more media
2 surfaces, a corresponding number of at least read devices, a
3 spindle motor for moving the one or more media surfaces, an
4 actuator for moving the at least read devices relative to the media
5 surfaces, a read device preamplifier, coupled to the number of at
6 least read devices, a servo control coupled to the actuator, for
7 driving the actuator in response to control signals, an integrated
8 data storage device controller integrated circuit comprising at
9 least one internal communications and control bus, for transferring
10 stored data and control data to and from elements within the
11 integrated data storage device controller and interconnected with
12 a host interface to transfer stored data and control data to and
13 from the integrated data storage device controller, a read device
14 data processor, coupled to the read device preamplifier and the at
15 least one internal communications and control bus, for receiving
16 and processing read device data from the read device preamplifier,
17 a motion control servo logic, coupled to the servo control, for
18 generating control signals for driving the servo control, a disc
19 controller, coupled to the at least one internal communications
20 bus, for transferring stored data to the host interface, and a

21 microcontroller, coupled to the at least one internal
22 communications bus, for generating control data to control devices
23 within the integrated data storage device controller integrated
24 circuit, a method of testing the integrated circuit data storage
25 device controller, comprising the step of:

26 selectively multiplexing outputs of one or more of the disc
27 controller, the microprocessor, and the read device data processor
28 with one or more I/O pins such that the integrated circuit may
29 selectively output signals from one or more of the disc
30 controller, the microprocessor, read device data processor.

1 31. The method of claim 30, wherein the data storage device
2 comprises an optical disc drive, the one or more media surfaces
3 comprises an optical disc, and the corresponding number of at least
4 read devices comprises a laser.

1 32. The method of claim 31, wherein the optical disc drive
2 comprises a CD-ROM drive and the optical disc comprises a CD-ROM.

1 33. The method of claim 31, wherein the optical disc drive
2 comprises a DVD drive, and the optical disc comprises a DVD.

1 34. The method of claim 31, wherein the optical disc drive
2 comprises a compact disc drive, and the optical disc comprises a
3 compact disc.

1 35. The method of claim 31, wherein the optical disc drive
2 comprises a CD-R drive, and the optical disc comprises a CD-R.

1 36. The method of claim 31, wherein the optical disc drive
2 comprises a CD-RW drive, and the optical disc comprises a CD-RW.

1 37. The method of claim 30, wherein the data storage device
2 comprises a floppy disk drive, the one or more media surfaces
3 comprises a magnetic floppy disk, and the corresponding number of
4 at least read devices comprises a read/write head.

1 38. The method of claim 30, wherein said step of selectively
2 multiplexing further comprises the step of:

3 selectively multiplexing outputs of the disc controller, the
4 microprocessor, and read device data processor with one or more I/O

5 pins such that the integrated data storage device controller
6 integrated circuit may selectively operate as a discrete disc
7 controller, component microprocessor, and read device data
8 processor.

1 39. In a tape drive having one or more media surfaces, a
2 corresponding number of at least read devices, a spindle motor for
3 moving the one or more media surfaces, a read device preamplifier,
4 coupled to the number of at least read devices, a servo control
5 coupled to the spindle motor for driving the spindle motor in
6 response to control signals, an integrated tape drive controller
7 integrated circuit comprising:

8 a host interface for interfacing with a host computer;

9 at least one internal communications and control bus, for
10 transferring stored data and control data to and from elements
11 within the integrated tape drive controller and interconnected with
12 the host interface to transfer stored data and control data to and
13 from the integrated tape drive controller;

14 a read device data processor, coupled to the read device
15 preamplifier and the at least one internal communications and
16 control bus, for receiving and processing read device data from the
17 read device preamplifier;

18 a motion control servo logic, coupled to the at least one
19 internal communications and control bus, and to the servo control,
20 for generating control signals for driving the servo control;

21 a disc controller, coupled to the at least one internal
22 communications bus, for transferring stored data to the host
23 interface; and

24 a microcontroller, coupled to the at least one internal
25 communications bus, for generating control data to control devices
26 within the integrated tape drive controller integrated circuit.

1 40. The integrated tape drive controller integrated circuit
2 of claim 39, wherein the tape drive controller integrated circuit
3 is rendered in complimentary Metal Oxide Semiconductor (CMOS)
4 transistor circuitry.

1 41. The integrated tape drive controller integrated circuit
2 of claim 39, further comprising:

3 a digital signal processor, coupled to the at least one
4 internal communications bus, for processing raw stored data from
5 the read device data processor and outputting processed stored
6 data.

1 42. The integrated tape drive controller integrated circuit
2 of claim 41, wherein said microcontroller comprises:

3 a microprocessor having a set of instructions for controlling
4 a tape drive; and

5 an internal memory for storing a first speed critical portion
6 of microprocessor code and data containing instructions for
7 processing, retrieving, and storing data to and from the tape
8 drive,

9 wherein the microprocessor accesses an external memory through
10 the at least one internal communications bus to access a second
11 non-speed critical portion of microprocessor code and data
12 containing instructions not related to processing, retrieving, and
13 storing date to and from the tape drive.

1 43. The integrated tape drive controller integrated circuit
2 of claim 42, wherein said at least one internal communications bus
3 comprises:

4 a microcontroller local bus coupled to said microprocessor and
5 said internal memory for transferring the microprocessor code and
6 data to and from the microprocessor;

7 a peripheral bus coupled to said microprocessor with said read
8 device data processor, said motion control servo logic, said disc
9 drive controller, and said digital signal processor;

10 an external memory bus, coupled to said microprocessor and an
11 external memory, for transferring microprocessor code and data to
12 and from said microprocessor; and

13 a bus/memory controller, coupled to and interfacing said
14 microcontroller local bus, said peripheral bus, and said external
15 memory bus.

1 44. The integrated tape drive controller integrated circuit
2 of claim 43, wherein a first portion of elements are provided as
3 hard design blocks, and a second portion of elements are provided
4 as soft design blocks such that the soft block components may be
5 readily redesigned without redesigning the hard block components in
6 order to customize the integrated tape drive controller integrated
7 circuit.

1 45. The integrated tape drive controller integrated circuit
2 of claim 39, wherein said internal communications bus further
3 comprises:

4 a MUX for selectively multiplexing outputs of one or more of
5 the disc controller, the microprocessor, and the read device data
6 processor with one or more I/O pins such that the integrated
7 circuit may selectively output signals from one or more of the of

8 the disc controller, the microprocessor, and the read device data
9 processor.

1 46. In a hard disk drive having one or more disk surfaces, a
2 corresponding number of read/write heads, a spindle motor for
3 rotating the disk surfaces, a voice coil motor for moving the heads
4 relative to the disk surfaces, a head preamplifier, coupled to the
5 number of read/write heads, a servo control coupled to the voice
6 coil motor for driving the voice coil motor in response to control
7 signals, an integrated hard disk drive controller integrated
8 circuit comprising at least one internal communications and control
9 bus, for transferring stored data and control data to and from
10 elements within the integrated hard disk drive controller and
11 interconnected with a host interface to transfer stored data and
12 control data to and from the integrated hard disk drive controller,
13 at least one of a read channel controller and a read/write channel
14 controller, coupled to the head preamplifier and the at least one
15 internal communications and control bus, for receiving and
16 processing read channel data from the head preamplifier, a motion
17 control servo logic, coupled to the servo control, for generating
18 control signals for driving the servo control, a disk controller,
19 coupled to the at least one internal communications bus, for
20 transferring stored data to the host interface, and

21 a microcontroller, coupled to the at least one internal
22 communications bus, for generating control data to control devices
23 within the integrated hard disk drive controller integrated
24 circuit, a method of testing the integrated circuit hard disk drive
25 controller, comprising the step of:

26 selectively multiplexing outputs of one or more of the disk
27 controller, the microprocessor, and the at least one of a read
28 channel controller and a read/write channel controller with one or
29 more I/O pins such that the integrated circuit may selectively
30 output signals from one or more of the disk controller, the
31 microprocessor, and the at least one of a read channel controller
32 and a read/write channel controller.

1 47. The method of claim 46, wherein said step of selectively
2 multiplexing further comprises the step of:

3 selectively multiplexing outputs of the disk controller, the
4 microprocessor, and the at least one of a read channel controller
5 and a read/write channel controller with one or more I/O pins such
6 that the integrated hard disk drive controller integrated circuit
7 may selectively operate as a discrete disk controller, component
8 microprocessor, and at least one of a read channel controller and
9 a read/write channel controller.

1 48. A method of testing an integrated circuit comprising a
2 plurality of predetermined circuit blocks corresponding to discrete
3 component circuits, said method comprising the step of:

4 selectively multiplexing outputs of one or more of the
5 plurality of discrete component circuit blocks with one or more I/O
6 pins such that the integrated circuit may selectively output
7 signals from one or more of the predetermined circuit blocks.

1 49. The method of claim 48, wherein said step of selectively
2 multiplexing further comprises the step of selectively multiplexing
3 outputs of one or more of the plurality of discrete component
4 circuit blocks with one or more I/O pins such that the integrated
5 circuit may selectively operate as discrete component corresponding
6 to one of the predetermined circuit blocks.